What is claimed is:

1. A phase-change memory device comprising:

a first conductive layer on a semiconductor substrate on a first level;

a second conductive layer on the semiconductor substrate on a second level, the second level being a different distance from the semiconductor substrate than the first level;

a phase-change memory layer that extends substantially parallel to a main surface of the semiconductor substrate and has a first surface facing the semiconductor substrate;

a first contact surface on the first surface of the phase-change memory layer to allow an electrical connection from the first conductive layer to the phase-change memory layer; and

a second contact surface on the first surface of the phase-change memory layer spaced apart from the first contact surface to allow an electrical connection from the phase-change memory layer to the second conductive layer.

2. The device of Claim 1, wherein the first contact surface provides for a flow of current from the first conductive layer to the phase-change memory layer and the second contact surface provides for a flow of current from the phase-change memory layer to the second conductive layer.

3. The device of Claim 1, further comprising a third conductive layer on the first level and spaced apart from the first conductive layer,

wherein the second contact surface is electrically connected to the second conductive layer through the third conductive layer.

4. The device of Claim 3, further comprising:

a first contact plug, which electrically connects the first contact surface and the first conductive layer; and

a second contact plug, which electrically connects the second contact surface and the third conductive layer.

5. The device of Claim 4, wherein the first contact plug and the second contact plug are on the semiconductor substrate on the same level.

6. The device of Claim 1, wherein the surface of the phase-change memory layer, except portions where the first contact surface and the second contact surface are provided, is covered with an insulating layer.

7. The device of Claim 1, wherein the second level is a greater distance from the substrate than the first level.

8. The device of Claim 1, wherein the phase-change memory layer is formed on the semiconductor substrate on a third level that is spaced a greater distance from the substrate than the first level.

9. The device of Claim 8, wherein the second level is spaced a greater distance from the substrate than the third level.

10. The device of Claim 1, wherein the phase-change memory layer includes a phase-change material layer containing chalcogen elements.

11. The device of Claim 1, wherein the phase-change memory layer includes a phase-change material containing chalcogen elements and a metal layer covering a surface of the phase-change material layer opposite the substrate.

12. The device of Claim 1, wherein the phase-change memory layer includes a material selected from the group consisting of Te, Se, Ge, any mixture thereof, and any alloy thereof.

13. The device of Claim 12, wherein the phase-change memory layer includes a material selected from the group consisting of Te, Se, Ge, Sb, Bi, Pb, Sn, As, S, Si, P, O, any mixture thereof, and any alloy thereof.

14. A phase-change memory device comprising:

a phase-change memory layer having a first surface facing a semiconductor substrate and a second surface which is opposite the first surface;

a plurality of conductive layers between the semiconductor substrate and the phase-change memory layer;

a plurality of contact plugs connected to the first surface of the phase-change memory layer such that the phase-change memory layer is electrically connected to ones of the plurality of conductive layers; and

an insulating layer, which covers the second surface of the phase-change memory layer.

15. The device of Claim 14, wherein the plurality of contact plugs include:

a first contact plug configured to apply an electric signal from a first conductive layer selected from the plurality of conductive layers to the phase-change memory layer; and

a second contact plug configured to apply an electric signal from the phase-change memory layer to a second conductive layer selected from the plurality of conductive layers.

16. The device of Claim 14, wherein the phase-change memory layer includes a phase-change material layer containing chalcogen elements.

17. The device of claim 14, wherein the phase-change memory layer includes a phase-change material containing chalcogen elements and a metal layer covering a surface of the phase-change material layer opposite the substrate.

18. A phase-change memory device comprising:

a lower electrode on a semiconductor substrate;

an upper electrode on the lower electrode;

a phase-change memory layer between the lower electrode and the upper electrode, the phase-change memory layer having a first surface adjacent the lower electrode;

a first contact plug connected to the first surface of the phase-change memory layer and configured to supply an electric signal from the lower electrode to the phase-change memory layer; and

a second contact plug connected to the upper electrode and the first contact plug.

19. The device of Claim 18, wherein the first contact plug and the second contact plug are connected to each other on a same level below the phase-change memory layer.

20. The device of Claim 19, wherein the first contact plug and the second contact plug are connected to each other by the lower electrode.

21. The device of Claim 18, wherein the phase-change memory layer is formed of a phase-change material layer containing chalcogen elements.

22. The device of Claim 18, wherein the phase-change memory layer includes a phase-change material containing chalcogen elements and a metal layer covering the top surface of the phase-change material layer.

23. The device of Claim 20, further comprising:

a second lower electrode on the substrate; and

a third contact plug that connects the second lower electrode to the phase-change material layer.

24. A phase change memory device comprising:

a phase-change memory layer on a semiconductor substrate, the phase-change memory layer having a major axis that is substantially parallel to a major axis of the semiconductor substrate and having a first surface and a second surface opposite the first surface that are substantially parallel to the major axis of the phase-change memory layer;

a first electrode on the semiconductor substrate that is electrically connected to the first surface of the phase-change memory layer in a first contact region of the phase-change memory layer; and

a second electrode on the semiconductor substrate that is electrically connected to the phase-change memory layer in a second contact region of the phase-change memory layer, the second contact region being space apart from the first contact region.

25. The device of Claim 24, wherein the second surface of the phase-change memory layer is opposite the substrate from the first surface of the phase-change memory layer.

26. The device of Claim 24, wherein the first surface of the phase-change memory layer is opposite the substrate from the second surface of the phase-change memory layer.

27. The device of Claim 24, wherein the first electrode is at a first level with respect to the substrate and the second electrode is at a second level with respect to the substrate, wherein the first level and the second level are different distances from the substrate.

28. The device of Claim 27, wherein the phase-change memory layer is at a third level with respect to the substrate, the third level being a distance from the substrate that is greater than a distance from the substrate of the first level and less than a distance from the substrate of the second level.

29. The device of Claim 28, further comprising a third electrode at a fourth level with respect to the substrate, the fourth level being a distance from the substrate that is less than the distance from the substrate of the third level, wherein the third electrode electrically connects the second electrode to the phase-change memory layer.

30. The device of Claim 24, wherein the first electrode and the second electrode are at a same level with respect to the substrate.

31. The device of Claim 24, wherein the phase-change memory layer comprises:

a phase-change material layer; and

a metal layer on the phase change material layer, the metal layer being on a surface of the phase-change material layer opposite the first and second contact regions.